



# Information Disclosure Statement By Applicant

Substitute for form 1449/PTO

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Application Number: 10/757,245

Filing Date: 01/14/2004

First Named Inventor: King

Art Unit: 2811

Examiner Name: N/A

Attorney Docket Number: PROG2000-1C2

Examiner Initials	Patent Number	Publication Date	Inventor Name
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

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